



## DV III : DSP processor board

### Technical Characteristics

Type	#	Description
FPGA I/O	100	FPGA SPARTAN 3.3V ( XILINX ® ) Typical program : <ul style="list-style-type: none"> <li>• 3 phase PWM modulator</li> <li>• Interface for an incremental encoder with 2 signals in quadrate and reference pulse</li> </ul> DSP bus is connected to the FPGA, 32 bits data/19 address lines
Binary I/O	8	Simple I/O
Analog IN	24	4x4 12bits, 1.65us conversion time simultaneous sampling 2x4 14 bits 2.4us conversion time, sim. Sampling +/- 10 or +/-5 V input range ( software selection ) 9/18 kohms
Analog OUT	8	10 bits Output range inside power supply, depending on the reference choosen
Serial	1 1	RS232 ( galvanic separation in option ) RS422
JTAG	1	DSP Debugging connector
DSP	32 bits 40 MHz 48 bits 2 Mbits 120 MFLOPS	Floating point processor Instruction execution rate Instructions word-length RAM
LINK	2	Processor link port ( see users manual of ADSP 210xx ). Connection of two processors for data exchange
Temperature	0-55°	Processor may be cooled for higher temperature range.
Dimensions	235x160x25	mm
Weight	235g	
Software Language	ANSI C	See ANALOG DEVICES documentation
Power	Single 5V	
FLASH	512kbyte	Retention of then program, FPGA program, User Data
EEPROM	4kbits	User Data
RAM	256kx48 bits	Program or Data memory 0 wait state
Watchdog		Protects the board against software failure